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A New Design Procedure for Optimization of Gain-boosted Cascode Amplifiers for High Speed Applications

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Abstract — **In order to reduce the design time of gain boosted cascode amplifier, a new and analytical design procedure for determining the component values and transistor dimensions of this amplifier is described. At first, this analytical design procedure is presented by the help of MOS square law equation and then it is explained for submicron processes in which square law equation is not valid. A design example is reported, finally**.

1 INTRODUCTION

Gain-boosted cascode amplifier (GBCA) is known as an excellent solution to the uneasy realization of the power optimized high-gain high-speed amplifiers. In this method the gain of initial cascode amplifier (ICA) is increased by the gain of an auxiliary amplifier or feedback amplifier (FA). However, the creation of a doublet pair in the transfer function of the main amp is a drawback for this method since it introduces a slow timing component in the amplifier settling time.

There have been some proposed design procedures for the optimum design of GBCA [1-3]. However, those are based on unwonted g_m/I_D methodology and EKV model [1] or MOS square law equation [2,3] which is not valid in submicron processes. Besides, those optimization methods are not free of some shortcomings [4].

In [4], after an exact analytical analysis, it is resulted that for optimum design of GBCA, the gain-bandwidth product (GBW) of FA should be within the 0.3 to half of the second pole frequency of ICA.

In this paper, based on the results of systematic analysis reported in [4], we describe a novel and analytical design procedure for determining the component values and transistor dimensions of GBCA. Our aim is to determine the W_1, L_1, W_2, L_2, W_3, L_3, I_B and I_F in Figure 1, for designing a GBCA with specific GBW, phase margin and gain and also optimizing the settling behavior of this amplifier in order to eliminate the slow timing component in transient response and get the minimum achievable settling time. For getting the best results with lower power dissipation, we choose all transistor channel lengths, L, as the minimum length available in the adopted technology.

In Section 2, we explain our analytical procedure by the help of MOS square law equation, then In Section 3, we explain our method for submicron processes. Section 4 contains a design example and Section 5 is conclusion.

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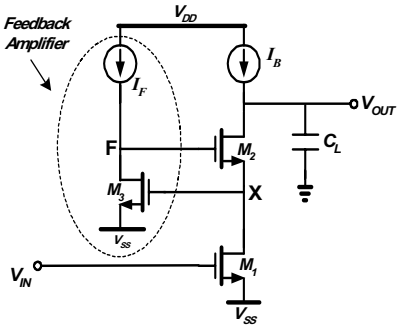

Figure 1: Gain-boosted cascode amplifier (GBCA).

2 DESIGN PROCEDURE BASED ON MOS SQUARE LAW EQUATION

MOS square law equation serves as the foundation for analog CMOS design, describing the dependence of drain current of transistor, I_D, upon the constant of technology such as, μC_{OX} and λ, the device dimensions, W and L, and the gate and drain potentials with respect to source.

$$I_D = \frac{\mu_n C_{OX}}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \quad (1)$$

In this section, by the help of this equation we describe our analytical design procedure.

Considering the results of the analytic analysis reported in [4], for optimum design of GBCA in high-speed applications, the GBW of FA, ω_u, should be within 0.3 to half of the frequency of the second pole of ICA. Since the FA and ICA are both single-stage amplifiers their GBW are as below:

$$\Omega_u = \frac{g_{m1}}{C_{OUT}} \quad (2)$$

$$\omega_u = \frac{g_{m3}}{C_F} \quad (3)$$

where Ω_u denotes the GBW of ICA, C_{OUT} and C_F denote the total capacitances at output node and node F, respectively, and g_m the transistor transconductance. For maximizing the bandwidth of the amplifier, the undesired parasitic poles should be driven to higher frequencies as much as possible.

The ICA is a two-pole amplifier with a dominant pole in output node, P_{OUT}, and a nondominat pole in node X, P_X. The value of P_X is:

$$P_X = \frac{g_{m2} + g_{mb2}}{C_X} = \frac{g_{m2}(1+\eta)}{C_X} \quad (4)$$

where g_{mb} and η denote the body-effect transconductance and coefficient respectively, and C_X is the total capacitance at node X. The value of C_X is:

$$C_X = 2C_{GD1} + C_{DB1} + C_{SB2} + C_{GS2} + C_{GS3} + C_{GD3} \quad (5)$$

The coefficient 2 is due to the Miller effect around the transistor M_1. If we ignore the small sidewall capacitance due to the width of diffusions, C_X is proportional to W_1, W_2 and W_3:

$$C_X = \alpha_1 W_1 + \alpha_2 W_2 + \alpha_3 W_3 \quad (6)$$

α_1, α_2 and α_3 are constants that their values depend on the process and layout methodology. At mean time, we ignore $\alpha_3 W_3$ in (6); we will prove the truth of this assumption at the end of this section. By experience, we know that M_1 and M_2 are not small transistors and therefore the layout of them are drawn by paralleling the m_1 and m_2 smaller transistors that their width are W_1/m_1 and W_2/m_2, respectively— multiple-gate fingers transistor layout. For the matching considerations, m_1 and m_2 are usually even numbers. Under these conditions, α_1 and α_2 are:

$$\alpha_1 = \frac{EC_j}{2} + C_{jsw} + C_{OV} \quad (7)$$

$$\alpha_2 = \frac{EC_j}{2} + C_{jsw} + C_{OV} + \frac{2}{3} L_2 C_{ox} \quad (8)$$

Where E, C_j, C_{jsw}, C_{OV} are diffusion width, junction capacitor, sidewall junction capacitor and gate-drain gate-source overlap capacitors, respectively. Regarding the square Law equation in MOS, the g_m of MOS transistor is proportional to the square root of its W.

$$g_m = \sqrt{2\mu_n C_{OX} \frac{W}{L} I_D} \quad (9)$$

As a result, P_X can be written as:

$$P_X = \frac{(1+\eta)\sqrt{(2\mu_n C_{OX} \frac{I_B}{L_2}) W_2}}{\alpha_1 W_1 + \alpha_2 W_2} \quad (10)$$

Regarding (10), by increasing W_2, both nominator and denominator of (10) increase. In a small W_2, by increasing W_2, increment in the nominator is more than the increment in denominator ,so P_X goes to higher frequencies. However, in a large W_2, by increasing W_2, increment in the nominator is less, as a result, P_X returns to lower frequencies. So there is a special value for W_2, which P_X is maximized.

Regarding the above discussion, there is an optimum value for W_2 with respect to each W_1. By differentiation of P_X with respect to W_2, a relationship results between W_1 and W_2 for maximizing P_X. That is:

$$\frac{\partial P_X}{\partial W_2} = 0 \Rightarrow W_2 = \frac{\alpha_1}{\alpha_2} W_1 = K W_1 \quad (11)$$

K is a process and layout related parameter, but it is usually about 0.1 to 0.5. Indeed, one of the main shortcomings in [3] is the assumption $W_1=W_2$. We prove that this is not a true assumption.

We can find another equation with respect to the desired phase margin. That is, for the phase margin of about φ_0, the ratio of P_X over Ω_u should be about $\tan(\varphi_0)$. That is:

$$\frac{P_X}{\Omega_u} = tan(\varphi_0) \Rightarrow \frac{\frac{g_{m2}(1+\eta)}{C_X}}{\frac{g_{m1}}{C_{OUT}}} = tan(\varphi_0) \quad (12)$$

$$\Rightarrow (1+\eta)\frac{g_{m2}}{g_{m1}} \frac{C_L + \alpha'_2 W_2}{\alpha_1 W_1 + \alpha_2 W_2} = tan(\varphi_0)$$

$\alpha'_2 W_2$ is a representation for the small parasitic capacitance due to the drain of M_2 at the output node. If we replace g_{m1} and g_{m2} with respect to (9), (12) simplifies to (13):

$$(1+\eta)\sqrt{\frac{W_2}{W_1}} \frac{C_L + \alpha'_2 W_2}{\alpha_1 W_1 + \alpha_2 W_2} = tan(\varphi_0) \quad (13)$$

(13) shows that phase margin adjustment is independent of I_B, and it should be done by changing the dimensions of transistors M_1 and M_2. Solving (11) and (13) with each other gives us W_1 and W_2. That is, W_1 and W_2 are:

$$W_1 = \frac{C_L}{\frac{2\sqrt{\alpha_1 \alpha_2}\, tan(\varphi_0)}{1+\eta} - \frac{\alpha_1 \alpha'_2}{\alpha_2}} \quad (14)$$

$$W_2 = K W_1 \quad (15)$$

The desired GBW, Ω_{u0}, is adjusted by solving (2) with respect to I_B. That is:

$$I_B = \frac{[\Omega_{u0}(C_L + \alpha'_2 W_2)]^2}{2\mu_n C_{OX} \frac{W_1}{L_1}} \quad (16)$$

Now, the optimum parameters for designing the cascode stage are determined. The only remained parameters are W_3 and I_F which are related to FA. Since the FA does not change the frequency response of ICA [1,3], the desired values for GBW and phase margin of the final amplifier are obtained.

The design of FA is not very hard. The only requirement to be satisfied is to adjust the gain and GBW of FA. In fact, a simple common source stage should be designed with the gain of $A_{V0}/(g_{m1}r_{O1}g_{m2}r_{O2})$ and a bandwidth of about 0.3 to half of P_X –since for optimum design of GBCA the GBW of FA should be about 0.3 to half of P_X [4]. Satisfying these conditions is not problematic, and this part of the design is a trivial work.

Now, we refer to the assumption that in (6) $\alpha_3 W_3$ is so smaller than $\alpha_1 W_1 + \alpha_2 W_2$. Since the GBW of FA should be about 0.3 to half of P_X and also for optimum

design of GBCA the GBW of ICA should be about 0.2 to 0.6 of P_X (The initial phase margin should be about 55º to 75º), so the GBW of FA and ICA should be in the same order. However, the load capacitance of FA is the parasitic capacitance that is seen in the gate of M_2 and is much lower than the load capacitance of ICA, C_L. As a result, g_{m3} should be much lower than g_{m1}. That is, the transistor M_3 is so smaller than M_1, and its parasitic capacitances are negligible compared with the parasitic capacitances due to M_1 and M_2, so we can simply ignore them.

3 DESIGN PROCEDURE IN SUBMICRON PROCESSES

Because of the short channel effects, the square law equation is not valid in submicron processes; therefore, the design procedure should not rely on it. Although, the design algorithm is similar to previous section, the optimum relations between the parameters will be found by some simple SPICE sweeps. In this section, we use a 0.25µm CMOS process for explaining the procedure.

Equation (11) states that the locus of maximum P_X's is in a determined value of W_2/W_1. Although, that equation is not exactly valid in submicron processes, the fact that there is an optimum value for W_2/W_1 is also true. The validity of this discussion is shown in Figure 3. In this figure, for different values of I_B and W_1, the locus of different P_X's is drawn versus W_2/W_1 ratio. Indeed, for this process, when the ratio of W_2/W_1 is about 0.15 to 0.25, P_X is in its maximum points, and this relationship is nearly independent of I_B and W_1. So, by a simple SPICE sweep of W_2 in arbitrary constant values for W_1 and I_B, and measuring relevant P_X's, the optimum ratio for W_2/W_1 will be determined.

Since by changing I_B, g_{m1} and g_{m2} nearly change by the same portion, adjustment of the desired phase margin is independent of I_B - this is a fact that can be deduced from (13) too. So, by sweeping W_1 in a constant and arbitrary value of I_B and keeping the ratio of optimum W_2/W_1 constant, the desired phase margin will be adjusted. Figure 4 proves this idea. In this figure, phase margin is swept for different values of I_B and W_1 when $W_2=0.15W_1$. By changing W_1 from 100µm to 500µm, phase margin changes 20 degrees, but by changing I_B from 50µA to 500µA, phase margin changes only 5 degrees. That is, for this example, the sensitivity of phase margin to W_1 is 8 times the sensitivity of phase margin to I_B.

Now, W_2 and W_1 are determined and by sweeping I_B the GBW of ICA will be adjusted. It is recommended that for getting better results, the previous algorithm for determining the optimum ratio of W_2/W_1, W_1 and I_B be repeated another time in the quiescent I_B resulted from first repeat of the algorithm.

Until now the ICA has been designed and by finding the total capacitance at the gate of M_2, designing the FA will begin –This capacitance can be found in the SPICE output file. The parameters for FA design are W_3 and I_F (or even L_3), and the design objectives are gain and GBW of FA.

We know the gain of ICA, $g_{m1}r_{O1}g_{m2}r_{O2}$. The rest of the desired gain should be provided by FA. Satisfying the gain requirement is not complicated. By decreasing I_F, increasing W_3 and L_3, or even by using cascode stage for FA, We can design a high gain FA. The key parameter for optimum design of GBCA for high-speed applications is the GBW of FA, ω_u.

The load capacitance of FA is the gate capacitance of M_2 and the drain capacitance of M_3. By increasing the W_3, g_{m3} and C_F increase, but at a small W_3, the increment in g_{m3} is higher than the increment in C_F- because in a small W_3, C_F is dominated by the gate capacitances of M_2.

However, in a large W_3, C_F is dominated by the drain capacitance of M_3, and the increment of C_F due to the increment in W_3 is higher than the increment in g_{m3}. Therefore, in a constant I_F, there is an optimum value for W_3 and by increasing W_3 we cannot increase ω_u more except by increasing I_F. Indeed, Because of the FA bandwidth requirement, there is a constraint on the minimum value of I_F. This fact is shown in Figure 5 obviously. For example, if the desired GBW of FA is 600 MHz, the I_F should not be lower than 10µA.

Summarizing, the design procedure is as following:

1) By sweeping W_2 for arbitrarily values of W_1 and I_B, the optimum ratio for W_2/W_1 is determined.
2) Considering above relation and sweeping W_1, the phase margin of the amplifier is adjusted.
3) By sweeping the I_B, the desired unity-gain frequency is adjusted.

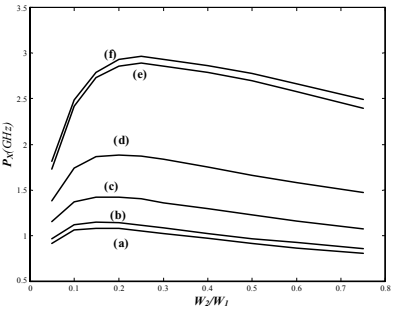

Figure 3: Locus of the second pole of ICA, P_X, versus W_2/W_1 when (a) I_B=50µA, W_1=100µm, (b) I_B=100µA, W_1=200µm, (c) I_B=100µA, W_1=150µm, (d) I_B=100µA, W_1=100µm, (e) I_B=100µA, W_1=50µm, (f) I_B=200µA, W_1=100µm

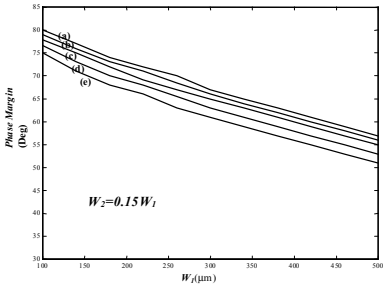

Figure 4: Phase margin versus W_1 when W_2=0.15W_1 and (a) I_B=50uA, (b) I_B=100uA, (c) I_B=200uA, (d) I_B=300uA, (e) I_B=500uA.

4) At meantime, the load capacitance and minimum desirable gain of the feedback amplifier is determined, so W_3 and I_F are determined from these requirements.

4 DESIGN EXAMPLE

In this section we give an example for our design procedure, our aim is to design a GBCA for the GBW of 300MHz, phase margin of 75°, and minimum gain of 80dB, in a 0.25μm CMOS process.

Firstly, by a simple sweeping of W_2 in arbitrary constant values for W_1 and I_B, and measuring relevant P_X's, the optimum ratio for W_2/W_1 will be determined. Based on the Figure 3 this ratio is 0.15 in this technology.

Secondly, for adjusting the phase margin about 75°, The W_1 is swept and the optimum ratio for W_2/W_1 is kept. The value of W_1 is found as 170μm, so W_2 will be 26μm.

Thirdly, for adjusting the GBW equal to 300MHz, by sweeping I_B, its suitable value is found as 100μA. Until now the ICA has been designed, the gain of this amplifier is 1400, the second pole, P_X, is at 1.2 GHz and the gate capacitance of M_2 is 40fF, which is the load capacitance of FA. Therefore, we should design a common source amplifier with the minimum gain

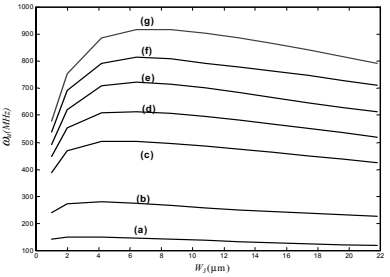

Figure 5: GBW of FA, ω_u, versus W_3 for various values of I_F, (a) I_F=2μA, (b) I_F=4μA, (c) I_F=8μA, (d) I_F=10μA, (e) I_F=12μA, (e) I_F=14μA, (e) I_F=16μA.

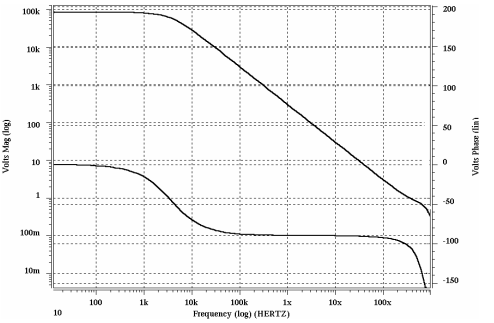

Figure 6: Frequency response of the designed GBCA

of 23 and the bandwidth of about 400MHz to 600MHz.

Finally for satisfying the FA requirements, we designed a common source amplifier with W_3=4μm and I_F=10μA. This results proves our assumption that the parasitic capacitance due to M_3 is negligible in node X. As a result of the above algorithm the *GBW*, phase margin and gain of the designed amplifier are 305MHz, 75degree and 98dB, respectively. The 0.01% settling time is about 6nSec without any slow timing component in it. The frequency response of this amplifier is shown in Figure 6.

5 CONCLUSION

An analytical design procedure based on the MOS square law equation was presented. Since this equation is not valid in submicron processes, a new design procedure based on some simple SPICE sweeps is reported. This procedure is very suitable for designing high-speed amplifiers and it reduces so much the design time of the gain-boosted cascode amplifiers, which has widespread usage in analog and mixed-mode circuit design.

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